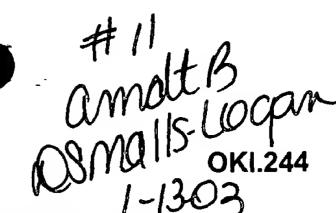
AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): Ken Ogura					Docket No. OKI.244	
Serial No. 09/883,363	1	ing Date e 19, 2001	Examiner H. Nguyen		Group Art Unit 2812	
Invention: CONDUCTOR POSTS, CONSTRUCTION FOR AND METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS USING THE CONDUCTOR POST, AND METHOD OF PROBING OF SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS						
TO THE ASSISTANT COMMISSIONER FOR PATENTS:  Transmitted in ewith is an amendment in the above-identified application.  The Replace been calculated and is transmitted as shown below.						
CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL	
TOTAL CLAIMS	13 -	24 =	0	x \$18	3.00 \$0.00	
INDEP. CLAIMS	2 -	5 =	0	x \$84	\$0.00	
Multiple Dependent Claims (check if applicable)						
<ul> <li>No additional fee is required for amendment.</li> <li>□ Please charge Deposit Account No. in the amount of         A duplicate copy of this sheet is enclosed.</li> <li>□ A check in the amount of to cover the filling fee is enclosed.</li> <li>☑ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0238         A duplicate copy of this sheet is enclosed.</li> <li>☑ Any additional filling fees required under 37 C.F.R. 1.16.</li> <li>☑ Any patent application processing fees under 37 CFR 1.17.</li> <li>□ Dated: December 30, 2002</li> </ul> ANDREW J. TELESZ, JR.  REG. NO. 33,581						
		TTE 150	on first class ma Assistant Co 20231.	ail under 37 (commissioner	ment and fee is being deposited with the U.S. Postal Service as C.F.R. 1.8 and is addressed to the for Patents, Washington, D.C.  on Mailing Correspondence  of Person Mailing Correspondence	





Date: December 30, 2002

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Ken Ogura

Group Art Unit: 2812

Serial No.: 09/883,363

Examiner: H. Nguyen

Filed: June 19, 2001

For: CONDUCTOR POSTS, CONSTRUCTION FOR AND METHOD OF

FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS USING THE CONDUCTOR POST, AND METHOD OF PROBING SEMICONDUCTOR

INTEGRATED CIRCUIT CHIPS

## <u>AMENDMENT</u>

Honorable Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

In response to the Office Action dated September 30, 2002, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

## In the Specification:

Replace the paragraph beginning on page 29 line 14 with the following paragraph:

An electrode pad 14, a first insulating layer 12, a first photosensitive material layer 60, and a seal member layer 64A are formed on an IC chip 10 shown in FIG. 24A in the same manner as the IC chip 10 of the first embodiment of the invention (See FIG. 1E). Then, as shown in FIG. 24B, the second photosensitive material layer 62 is

